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Terms used **model to hardware correlation** Found **5** of **852,541**

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Results 1 - 5 of 5

Relevance scale

1 New perspectives in physical design: Uncertainty-aware circuit optimization

Xiaoliang Bai, Chandu Visweswariah, Philip N. Strenski

June 2002 **Proceedings of the 39th conference on Design automation**

Full text available: pdf(131.43 KB) Additional Information: full citation, abstract, references, citings, index terms

Almost by definition, well-tuned digital circuits have a large number of equally critical paths, which form a so-called "wall" in the slack histogram. However, by the time the design has been through manufacturing, many uncertainties cause these carefully aligned delays to spread out. Inaccuracies in parasitic predictions, clock slew, model-to-hardware correlation, static timing assumptions and manufacturing variations all cause the performance to vary from prediction. Simple statistical princip ...

Keywords: circuit tuning, nonlinear, optimization, performance optimization, process variation, small uncertainty, transistor sizing

2 Block-based Static Timing Analysis with Uncertainty

Anirudh Devgan, Chandramouli Kashyap

November 2003 **Proceedings of the 2003 IEEE/ACM international conference on Computer-aided design**

Full text available: pdf(181.39 KB) Additional Information: full citation, abstract, index terms

Static timing analysis is a critical step in design of any digitalintegrated circuit. Technology and design trends have ledto significant increase in environmental and process variationswhich need to be incorporated in static timing analysis.This paper presents a new, efficient and accurate block-basedstatic timing analysis technique considering uncertainty.This new method is more efficient as its modelsarrival times as cumulative density functions (CDFs) anddelays as probability functions (PDFs ...

3 Design automation methodology and rf/analog modeling for rf CMOS and SiGe BiCMOS technologies

D. L. Harame, K. M. Newton, R. Singh, S. L. Sweeney, S. E. Strang, J. B. Johnson, S. M. Parker, C. E. Dickey, M. Erturk, G. J. Schulberg, D. L. Jordan, D. C. Sheridan, M. P. Keene, J. Boquet, R. A. Groves, M. Kumar, D. A. Herman, B. S. Meyerson

March 2003 **IBM Journal of Research and Development**, Volume 47 Issue 2-3

Additional Information: full citation, abstract, references, index terms

The rapidly expanding telecommunications market has led to a need for advanced rf

integrated circuits. Complex rf- and mixed-signal system-on-chip designs require accurate prediction early in the design schedule, and time-to-market pressures dictate that design iterations be kept to a minimum. Signal integrity is seen as a key issue in typical applications, requiring very accurate interconnect transmission-line modeling and RLC extraction of parasitic effects. To enable this, IBM has in place ...

4 Low-power circuits and technology for wireless digital systems

S. V. Kosonocky, A. J. Bhavnagarwala, K. Chin, G. D. Gristede, A.-M. Haen, W. Hwang, M. B. Ketchen, S. Kim, D. R. Knebel, K. W. Warren, V. Zyuban

March 2003 **IBM Journal of Research and Development**, Volume 47 Issue 2-3

Additional Information: full citation, abstract, references, citings, index terms

As CMOS technology scales to deep-submicron dimensions, designers face new challenges in determining the proper balance between aggressive high-performance transistors and lower-performance transistors to optimize system power and performance for a given application. Determining this balance is crucial for battery-powered handheld devices in which transistor leakage and active power limit the available system performance. This paper explores these questions and describes circuit techniques fo ...

5 Coping with variability: the end of deterministic design: Death, taxes and failing chips

Chandu Visweswariah

June 2003 **Proceedings of the 40th conference on Design automation**

Full text available: pdf(145.71 KB) Additional Information: full citation, abstract, references, citings, index terms

In the way they cope with variability, present-day methodologies are onerous, pessimistic and risky, all at the same time! Dealing with variability is an increasingly important aspect of high-performance digital integrated circuit design, and indispensable for first-time-right hardware and cutting-edge performance. This invited paper discusses the methodology, analysis, synthesis and modeling aspects of this problem. These aspects of the problem are compared and contrasted in the ASIC and custom ...

Keywords: Statistical timing, design methodology, parametric yield prediction

Results 1 - 5 of 5

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Please review the Quick Tips below or for more information see the Search Tips.

Quick Tips

- Enter your search terms in lower case with a space between the terms.

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  sales offices
  ```

  You can also enter a full question or concept in plain language.

  ```
  Where are the sales offices?
  ```

- Capitalize proper nouns to search for specific people, places, or products.

  ```
  John Colter, Netscape Navigator
  ```

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  ```
  "museum of natural history" "museum of modern art"
  ```

- Narrow your searches by using a + if a search term must appear on a page.

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  museum +art
  ```

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  ```
  museum -Paris
  ```

Combine these techniques to create a specific search query. The better your description of the information you want, the more relevant your results will be.

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museum +"natural history" dinosaur -Chicago
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("design validation" <in> ti)
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('design validation' <in> ti) Search

Check to search within this result set

Results Key:
JNL = Journal or Magazine **CNF** = Conference **STD** = Standard

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Schmaltz, D.; Harris, G.F.; Yogananadan, N.; Pintar, F.; Sances, A., Jr.;
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```
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<or> (design <near/1>
verif*)) <and> remov*
```

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((design <near/1> valid*) <or> (design <near/1> veri Search

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Results Key:
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Example: optical <and> (fiber <or> fibre) <in> ti
3) Limit the results by selecting Search Options.
4) Click Search. See Search Examples

```
((design <near/1> valid*)
<or> (design <near/1>
verif*)) and (remov* <near/5>
defect* <near/5> data)
```

Start Search Clear

Note: This function returns plural and suffixed forms of the keyword(s).

Search operators: <and> <or> <not> <in> More

Field codes: au (author), ti (title), ab (abstract), jn (publication name), de (index term) More

Search Options:

Select publication types:

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Organize search results by:

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List 15 Results per page

Your search matched **2** of **1138071** documents.
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Refine This Search:
You may refine your search by editing the current search expression or enteri new one in the text box.

((design <near/3> valid*) <or> (design <near/3> veri Search

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Results Key:
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1 **Cleanroom software engineering-plan your work and work your plar small increments**
Spangler, A.;
Potentials, IEEE , Volume: 15 , Issue: 4 , Oct.-Nov. 1996
Pages:29 - 32

[Abstract] [PDF Full-Text (1080 KB)] IEEE JNL

2 **Emulation-based design errors identification**
Castelnuovo, A.; Fin, A.; Fummi, F.; Sforza, F.;
Defect and Fault Tolerance in VLSI Systems, 2002. DFT 2002. Proceedings. 1
IEEE International Symposium on , 6-8 Nov. 2002
Pages:365 - 371

[Abstract] [PDF Full-Text (895 KB)] IEEE CNF

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Check to search within this result set

Results Key:
JNL = Journal or Magazine **CNF** = Conference **STD** = Standard

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1 **Functional test generation for full scan circuits**
Pomeranz, I.; Reddy, S.M.;
Design, Automation and Test in Europe Conference and Exhibition 2000. Proceedings , 27-30 March 2000
Pages:396 - 401

[Abstract] [PDF Full-Text (40 KB)] **IEEE CNF**

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2 **Proceedings International Test Conference 2000 (IEEE Cat. No.00CH37159)**

Test Conference, 2000. Proceedings. International , 3-5 Oct. 2000
[Abstract] [PDF Full-Text (544 KB)] **IEEE CNF**

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3 **RTL-based functional test generation for high defects coverage in di SOCs**
Santos, M.B.; Goncalves, F.M.; Teixeira, I.C.; Teixeira, J.P.;
European Test Workshop, 2000. Proceedings. IEEE , 23-26 May 2000
Pages:99 - 104

[Abstract] [PDF Full-Text (508 KB)] **IEEE CNF**

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4 **Proceedings 18th IEEE VLSI Test Symposium**

VLSI Test Symposium, 2000. Proceedings. 18th IEEE , 30 April-4 May 2000
[Abstract] [PDF Full-Text (728 KB)] **IEEE CNF**

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5 **Validating fault tolerant designs using laser fault injection (LFI)**
Samson, J.R., Jr; Moreno, W.; Falquez, F.;
Defect and Fault Tolerance in VLSI Systems, 1997. Proceedings., 1997 IEEE

International Symposium on , 20-22 Oct. 1997
Pages:175 - 183

[Abstract] [PDF Full-Text (684 KB)] IEEE CNF

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6 **A method for the evaluation of behavioral fault models**
Gaudette, E.; Moussa, M.; Harris, I.G.;
High-Level Design Validation and Test Workshop, 2003. Eighth IEEE International , 12-14 Nov. 2003
Pages:169 - 172

[Abstract] [PDF Full-Text (379 KB)] IEEE CNF

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7 **Software-based self-test methodology for crosstalk faults in proces**
Xiaoliang Bai; Li Chen; Dey, S.;
High-Level Design Validation and Test Workshop, 2003. Eighth IEEE International , 12-14 Nov. 2003
Pages:11 - 16

[Abstract] [PDF Full-Text (524 KB)] IEEE CNF

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8 **Proceedings International Test Conference 2002 (Cat. No.02CH3738**

Test Conference, 2002. Proceedings. International , 7-10 Oct. 2002
[Abstract] [PDF Full-Text (545 KB)] IEEE CNF

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9 **RTL design validation, DFT and test pattern generation for high defe coverage**
Santos, M.B.; Gonqalves, F.M.; Teixeira, I.C.; Teixeira, J.P.;
Test Workshop, IEEE European, 2001 , May 29 - Jun. 1, 2001
Pages:99 - 105

[Abstract] [PDF Full-Text (560 KB)] IEEE CNF

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10 **International Test Conference 1999. Proceedings (IEEE Cat. No.99CH37034)**

Test Conference, 1999. Proceedings. International , 28-30 Sept. 1999
[Abstract] [PDF Full-Text (600 KB)] IEEE CNF

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11 **Proceedings International Test Conference 1998 (IEEE Cat. No.98CH36270)**

Test Conference, 1998. Proceedings. International , 18-23 Oct. 1998
[Abstract] [PDF Full-Text (660 KB)] IEEE CNF

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12 **I_{DDQ} testing and defect classes-a tutorial**
Soden, J.M.; Hawkins, C.F.;
Custom Integrated Circuits Conference, 1995., Proceedings of the IEEE 1995 , May 1995
Pages:633 - 642

[Abstract] [PDF Full-Text (956 KB)] IEEE CNF

13 **A methodology for rapid prototyping of real-time image processing systems**

Kralijic, I.C.; Quenot, G.M.; Zavidovique, B.;

Rapid System Prototyping, 1995. Proceedings., Sixth IEEE International Work: on , 7-9 June 1995

Pages:97 - 103

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... :absolute;top:5141;left:470"><nobr>**model to hardware correlation**, ...
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... **model-to-hardware correlation** at different points in the. process distribution. Other parameters of interest are voltage range ...
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[PDF] The I/O Power Supply Modeling For Pentium 4 Microprocessor Packaging
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... 6. REFERENCES. [1] S. Chun, L. Smith, R. Anderson, M. Swaminathan, "**Model to**

hardware correlation for power distribution induced ...
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... M, v, **Daniel COOPS** was christened on 16 Dec 1827 in Knutsford. [Notes]. F, vi, Harriet COOPS was christened on 30 May 1830 in TOFT. [Notes] ...
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